# XTRP Databoard Sign-off

- "Production" XTRP Databoards were produced in Summer '00
  - found to have problems with cracked/broken vias
  - ultimately traced (much later) to a drilling problem in fabrication
    - no organic coatings, aspect ratio good

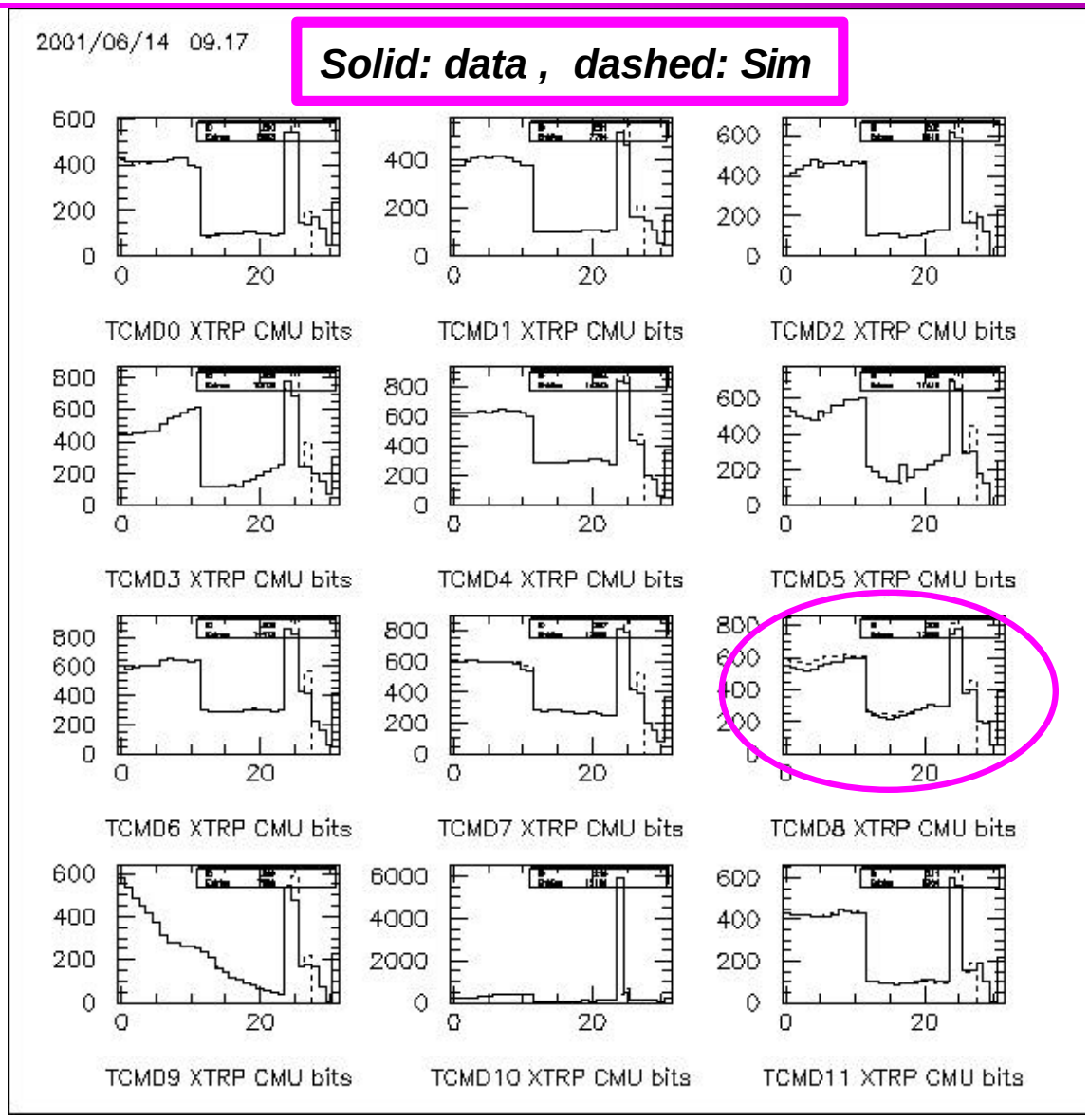
- Between November '00 and March '01, worked ***very*** hard to get the boards in shape for the run
  - we knew that even if we built new boards, we had to get these working
  - significant technician support from Fermilab

- Currently, the boards are working and we are happy with the functionality (but not happy with the reliability) and we are ready to build new boards

# XTRP Update

## XTRP Status

- All 12 boards in and working
- Currently:
  - 6 masked segments (/288)
  - calorimeter and muon paths show good agreement
  - handful of hot/stuck bits (mostly IMU path)
- Problems:
  - bunch counter mismatches
  - data/sim mismatches (<1%)
    - bit errors from bad vias
  - lack of fully functional spares
- We will continue to fight bit problems until we get new boards.



# What Has Happened

- Incorporated ECO's into new layout
  - most changes had to do with bit ordering
    - (*e.g.* we got the adjacent wedge cal bits backwards)
  - ***ALL*** changes were "local" layout changes, the fundamental board layout stays the same
    - crucial point, since we have seen no timing problems (33ns clocks)
  - everything backwards compatible, can run new boards with old
  - independent verification of all layout changes (2nd pair of eyes)
- Understood what went wrong with the previous boards
  - important to insure it won't happen again
- Underwent an engineering review of the new boards (and via problems)

# XTRP Databoard Review

- Date: 7-Jun-01
- Reviewers:
  - Bob DeMaat, Rick Van Berg, Boris Baldin
- We went over:
  - the history of the boards
  - what went wrong
  - what we can (and will) do to prevent it with the new version
- Peter collected reviewers comments
  - executive summary: we are doing the right things.

# XTRP Databoard Sign-off

- **Question:** Are there any “features” of the current version of the boards/system that are untested and we might want to incorporate into a new layout?

- Outstanding (non-via) issues: *(this is as close as I get to full-disclosure)*
  - bunch counter mismatches: FPGA problem
  - Track Trigger interface: we believe it works, although it has not been as extensively tested as the CAL and muon paths.
  - CMU crack bits: we believe they work, but we haven’t paid close attention to them. If there are any problems, they can be fixed in the maps.
  - Level 2 interface: works, largely FPGA driven

- Relatively small system, would rather proceed with production now and have to put a few wires on 15 boards than wait 6 months to build more.

- ***Goal:*** 15 new, fully functional boards installed during the fall shutdown.

# Status

- Parts have been ordered, most are in-hand.
  - Some components out of production, but we were able to get what we need.
- Board fabrication beginning now.
  - Vendor: Ambitech (they did ADMEMs, they did NOT do XTRP boards)
  - 3 week turn around on boards
- We will do via tests (sample) in Urbana before assembly
- Assembly turn-around time is 3 weeks.
- Assembled boards in Urbana by end of August.
- ***Goal:*** 15 new, fully functional boards installed during the fall shutdown.